ISAAC -- Integrated Silicon Automotive Accelerometer

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SUMMARY

The pervasiveness of automotive passive restraint systems has emphasized the need for improving system reliability while simultaneously reducing the cost and size of the system. This paper describes an accelerometer that utilizes silicon micromachining in a dissolved wafer process and a CMOS ASIC along with low cost plastic packaging to support the requirements of the next generation of automotive passive restraint systems.

INTRODUCTION

Automotive passive restraint systems are evolving from the current "distributed" systems in which several acceleration sensitive switches are placed near the front of the vehicle to more sophisticated "single-point" systems that use an accelerometer and a microprocessor-based algorithm in a module located in the passenger compartment. These single-point systems provide improved reliability through part count reduction and simplified wiring while at the same time lowering system costs. This paper presents a unique approach to these systems in the application of micromachined sensor technology.

Single-point passive restraint systems have specific requirements that, if taken into consideration, can allow system partitioning and selection of accelerometer technologies and designs that result in lower overall system cost. Algorithms that are used to make deployment decisions typically use at a minimum, change in velocity and peak acceleration data. Acceleration signals in the 50 g range with a response of up to 400 Hz are typically

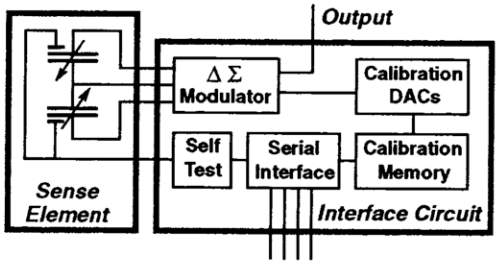

Figure 1. The block diagram of the ISAAC.

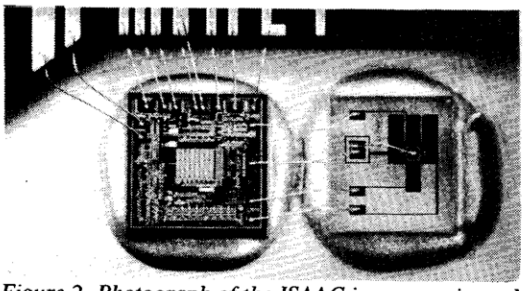

Figure 2. Photograph of the ISAAC in a ceramic package before lid seal.

the signals of interest. These acceleration signals must be continuously evaluated without placing undo demands on the system microprocessor.

Since the system must be reliable for over the full service life of the vehicle, a self test feature which checks the mechanical integrity and stability of the accelerometer is of primary importance. These application specific requirements, along with design for manufacturability considerations, have been instrumental in the technology selection for this low-cost accelerometer.

OVERVIEW OF THE SENSOR

The Integrated Silicon Automotive Accelerometer (ISAAC) is a two-chip accelerometer that consists of a differential, capacitive micromachined sense element die assembled in an IC package along with a CMOS interface chip containing EEPROM calibration circuits (Figs. 1 and 2). The sense element chip generates a differential, femtofarad-level signal that is fed to the interface chip via bond wires. The interface chip uses a delta-sigma circuit to convert the sense element signals into a pulse density modulated output that is proportional to the applied acceleration.

The interface chip has EEPROM and digital circuitry that allows the gain and offset of the completed device to be trimmed to the desired specification. A serial interface allows the ISAAC to communicate with a microprocessor to facilitate accelerometer calibration during device manufacture, and to facilitate a secure self test activation after the device is installed in a vehicle.

A modular two-chip approach was selected for this device to allow the interface circuit technology and the sense element technology to evolve independently of each other. This has been instrumental in allowing rapid development times since enhancements made to one die can be incorporated into the accelerometer without affecting the other die.

This modular approach to ISAAC is also evident in the packaging technologies selected for the device. Initially, multilayer ceramic technology was used. It has currently been replaced with molded plastic package technology which supports many body styles and lead configurations while lowering overall sensor cost.

SENSE ELEMENT DIE

The sense element chip uses a glass substrate and a single-crystal silicon torsional microstructure with differential mass. It has a central "pedestal" support with capacitive plates and an electrostatic self test mechanism [1]. The single-crystal silicon has material properties that are highly repeatable and this enhances the manufacturability of the device.

The central pedestal support greatly reduces the susceptibility of the sensor to die stresses since it isolates the microstructure from the substrate. This eases packaging constraints and also improves the manufacturability of the sensor. The central pedestal also incorporates a buried contact to connect the microstructure to the common mode potential of the interface circuit.

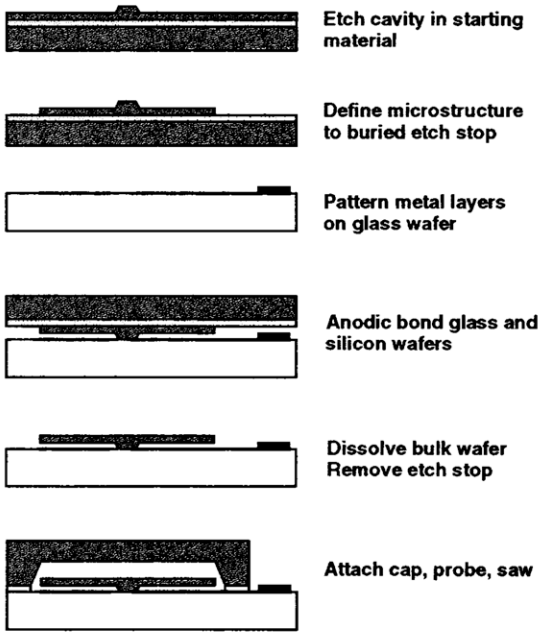

Figure 3. Simplified process flow for the ISAAC sense element die.

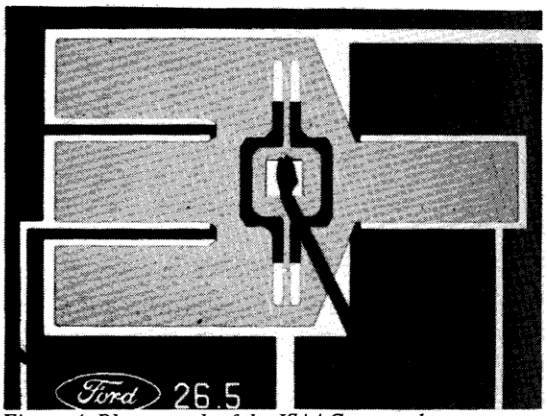

Figure 4. Photograph of the ISAAC sense element.

The device is fabricated by starting with a silicon wafer that has an etch stop buried below an epitaxial layer. This epitaxial layer is patterned and etched to create what will become the capacitive gap of the sense element. The remaining epi layer is patterned to form the outline of the final microstructure. A pyrex glass wafer is then patterned with conductors to form the fixed plates of the capacitors as well as the self test electrodes and bond pad regions. The two wafers are then electrostatically bonded together. During the bonding process, the central pedestal makes physical contact with the metal on the glass wafer. This trace is connected to the common mode potential of the interface chip.

After the wafers are bonded together, the bulk wafer is removed down to an etch stop layer. This etch stop layer is then removed using a selective etching process. A second silicon wafer is then patterned and etched to form a cap. Dielectric materials are used to insulate the traces that feed through from the enclosed cavity to a shelf on the glass wafer that contain pads for wirebonding. The dielectric materials also aid in forming a hermetic seal between the glass substrate and the silicon cap. At this point, the wafers are ready for probe test and wafer saw.

The sense element chip provides a differential capacitive output as illustrated in the left side of Fig. 5. Typical values for the capacitance at zero acceleration are 150fF while full scale acceleration results in approximately a 15fF change to both C_A and C_B. This capacitive output is a nonlinear function of acceleration. The interface circuit linearizes the response by implementing the function shown in the right side of Fig. 5.

Dimensioning of the air gaps, torsion beams and damping holes creates a mechanical microstructure that is overdamped thus providing an antialias filter for the

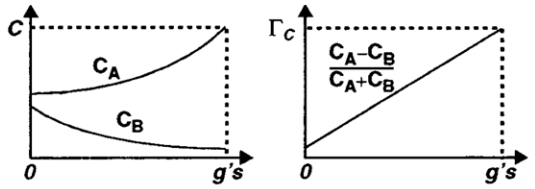

Figure 5. Representation of capacitance and Γ_C as a function of acceleration for the ISAAC sense element.

sampled-data interface circuit. The -3db frequency response is 400Hz at room temperature while the resonant frequency of the micromechanical structure is 2.7KHz. The viscosity of the gas constituents surrounding the microstructure directly influence the damping and there is a temperature coefficient associated with this. For accelerometers used in passive restraint systems however, these changes in damping are acceptable.

The sense element chip incorporates an active self test feature that allows the micromechanical device to be electrostatically deflected in a manner that mimics the mechanical response of the device during acceleration. During normal operation, the self test electrode is held at the common mode potential. During self test, the interface chip generates a self test voltage that is applied to this node via a bond wire.

The silicon cap is used in combination with the glass substrate to provide the hermetic package function at the wafer level. This cap provides electrostatic shielding as well as an enclosure that protects the microstructure from contamination or from changes in gas constituents. It also provides protection from the plastic mold compound used in accelerometer packaging.

INTERFACE CIRCUIT

The interface circuit is fabricated in a 1.6 micron CMOS process with EEPROM. The primary function of this circuit is to convert the femtofarad-level capacitance signals from the sense element to a pulse signal

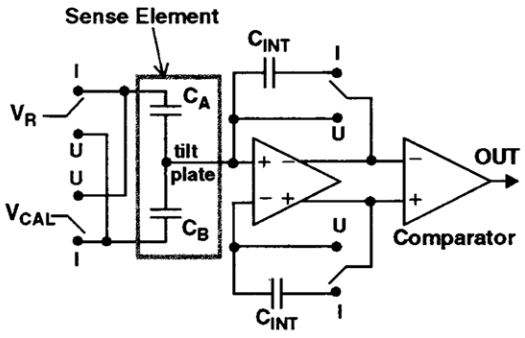

Figure 6. Delta Sigma circuit showing unity and integrate switches and the calibration voltage node.

suitable for digital signal processing. The chip also provides compensation for sensor offset and sensitivity variations while providing a self test and reset function. Design considerations for the circuit include stability over voltage and temperature variations with low power and low cost also being primary factors.

The interface chip implements an open-loop "charge-mode" delta-sigma modulator using an internal 250KHz clock. The delta sigma modulator is clocked between a "unity phase" which nulls amplifier inputs and an "integrate phase" during which the sense element signal is evaluated and the output state is determined. The calibration voltages (V_{CAL}) that are applied to the sense element are a function of both the clock phase and the polarity of the output signal which is latched at the end of each clock phase. Since acceleration-induced capacitance changes occur very slowly compared to the clock period, the values of $C_A$and C_B are essentially constant during any given clock cycle.

Sense element capacitances C_A and C_B are inherently nonlinear as shown qualitatively in Figure 5. However the difference of these capacitances divided by their sum is substantially more linear with respect to acceleration and this quantity is defined as:

$$\Gamma_C = \frac{C_A - C_B}{C_A + C_B} \tag{1}$$

It is thus desirable to develop a circuit that uses the function defined by Γ_C as a factor in the gain term such that the output is described by:

$$FPD = B + G(\Gamma_C) \tag{2}$$

where the sensitivity calibration term G, and the offset calibration term B, depend only on two sensor calibration codes and fixed reference voltages. The FPD, fractional output pulse density, is defined as the number of clock periods per second having a high OUT value, divided by the clock frequency. The circuit described in Figure 6 implements these functions and has been described in detail elsewhere [2].

The two calibration codes are stored in EEPROM and these are used to generate the calibration voltages V_{CAL}. Tap points from an on-chip 9-bit resistor string DAC are selected by these 9-bit calibration codes. The EEPROMs driving the DACs are programmed during the final step of ISAAC manufacture, thus allowing cancelation of the variations in die fabrication and packaging processes that might impact device performance.

The interface circuit contains a serial peripheral interface (SPI) that allows the accelerometer to communicate directly with a microprocessor. The SPI interface

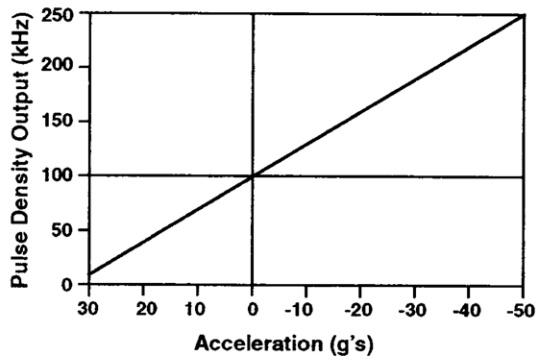

Figure 7. DC acceleration transfer characteristic of the accelerometer.

is used for two primary functions 1) to allow calibration values to be loaded into the sensor and 2) to allow a microprocessor to issue commands to the accelerometer to reset the device and to activate the self test mechanism. The accelerometer can also be configured in a mode that allows the self test and reset to be controlled directly by changing the voltage on the associated pin. This allows the sensor to be used in systems that do not support SPI communications.

PACKAGING

The packaging technology for ISAAC is driven by four primary considerations 1) facilitate the use of low-cost, reliable plastic IC assembly and molding processes for high volume manufacturing, 2) support for standard lead configurations and body size to simplify automated handling and placement on the airbag module substrate, 3) the package must orient the die so that the axis of sensitivity is parallel to the module mounting surface and 4) the package must isolate the die and bond wires from contamination or mechanical stresses while providing electrical connection between the die and the PCB traces.

While the initial ISAAC prototypes were configured in ceramic side-braze dual-in-line packages, current devices are packaged in an epoxy-based transfer molded package in a SIP configuration. Conventional epoxy die attach and gold wirebonding processes are used to assemble the accelerometer. An SMD package is currently under development.

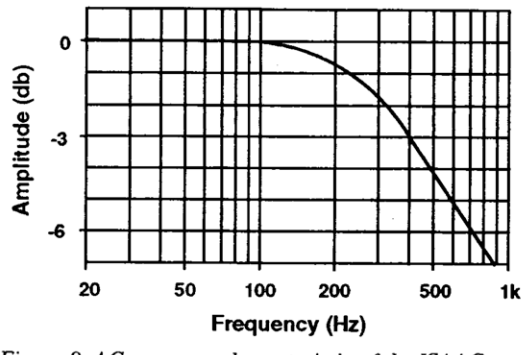

Figure 8. AC response characteristic of the ISAAC.

ISAAC Performance Summary
(Over all conditions)

Range	+30 to -50 g
Sensitivity	3 kHz/g
Offset	100 kHz
-3db Frequency	400 Hz
Power Supply	<2 mA @ 5V
Cross Axis	<2% FSO
Linearity	<2% FSO
Self Test	15 g's

RESULTS

The DC performance of the ISAAC is shown in Fig. 7 although the offset and gain are programmable over a wide range through the EEPROM. The AC response is shown in Fig. 8 which demonstrates the overdamped nature of the microstructure. These parameters have been specifically chosen to meet the requirements of automotive systems in a very cost effective manner. The results of other functional testing is shown in the table above.

The ISAAC crash sensor meets all automotive reliability specifications including shock survivability, temperature cycling, vibration endurance, life and retention testing, ESD and latch-up.

Substantial vehicle-level testing of the accelerometer at the crash barrier, along with fleet testing in "flight recorder" systems is verifying the suitability of the ISAAC technology for automotive passive restraint systems.

CONCLUSION

The accelerometer described in this paper incorporates precision circuitry, EEPROM calibration and full mechanical self test, to provide superior performance in the automotive environment. It has been designed for a specific system application in a modular way that promotes continued technology improvement, enhanced manufacturability, and continued cost reduction.

REFERENCES

[1] J. Cole, "A New Sense Element Technology for Accelerometer Subsystems," Transducers '91, June 24-27, 1991, pp 93-96.

[2] C. Kemp and L. Spangler "An Accelerometer Interface Circuit" *1995 Custom IC Conference*, May 1-4, 1995.