



CASE STUDY

Au Flip Chip and TSV Interposer for Phased-Array Antenna Systems

Design the package and assembly process to produce components for a SiGe chips in a phased array antenna system.



BACKGROUND: Phased-array antennas provide the ability to beamsteer by adjusting the phase of the signal from different elements of an array of individual antennas. Based on these slight differences in phase, the beam energy is maximized in directions where amplitudes combine and it is minimized in undesired directions. Packaging the gain circuits as close to the antenna radiator as possible improves performance and allow miniaturization the entire system. This type of compact assembly creates a number of challenges that must be overcome to create functioning phased array antenna systems.

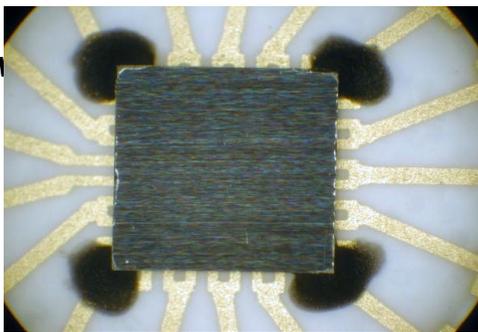
Project Details: The customer, a long time manufacturer of phased array systems, was developing a new architecture for operation in the Ka and Ku bands. The packaging plan called for custom SiGe chips to be flip chip attached in an array on a substrate. Low impedance electrical connections along with robust mechanical attachment were necessary for the 20 to 30 connections that each chip needed to make to the substrate. The system requirement also included the ability to “tile” the flip chip die into a tightly package array. Finally, since the SiGe chips were directly driving the antenna array, and since the array was to operate in an outdoor environment,

the periphery of the flip chip array needed to be hermetically sealed, not only for environmental robustness, but also to ensure contamination did not impact the electrical performance of the array.

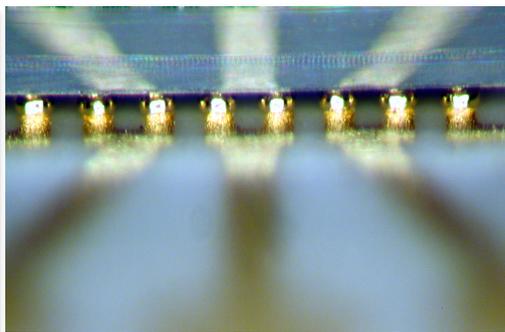
Initial assemblies by the customer’s traditional supplier were fabricated with a gold stud-epoxy flip chip process. Not only did these parts not pass performance requirements, they also broke with the slightest bit of shock. After analyzing the possible alternatives, a Au-Au

By analyzing the functional requirements as well as the system operating conditions, a gold-gold flip chip arrangement with integral seal rings was proposed. This approach promised not only provided excellent electrical performance, but it also significantly more robust devices. A variety of design options were analyzed with both physical and electrical modeling as well as through a set of experiments. The ability to stud bump individual die and to flip chip attach them onto larger substrates allowed for a wide range of designs to be considered.

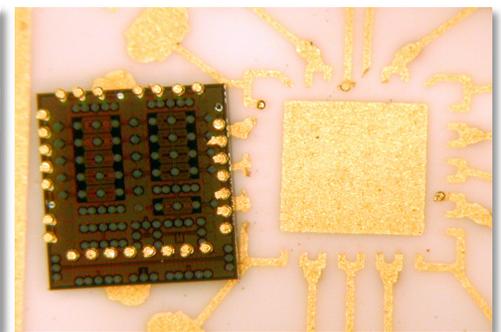
For the first round of experiments, Au thick film on ceramic test substrates were fabricated along with corresponding silicon test chips. Both the test die and Au traces on the ceramic substrate were Au stud bumped.



A test chip that was physically separated showing the strength of the flip chip bonds



A side view of the Au-Au thermocompression flip chip die assembly



A silicon test chip thermocompression bonded to a ceramic substrate

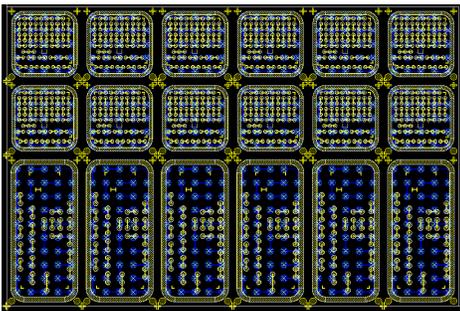
The Au-Au flip chip thermocompression process was developed and devices were fabricated and tested. The devices passed the electrical test requirements and were then subjected to a full battery of reliability stress tests, after which they were again electrically tested. The devices showed no degradation in electrical performance after the stress tests. Devices were then shear tested and failure was observed in either the thick film material or in the die substrate. No failures were observed in the flip chip bumps themselves.

Based on the success of the first set of experiments, a second round of devices were designed and fabricated to evaluate the incorporation of a hermetic seal ring along with the flip chip bumps. The array size, seal ring width and radius were varied to understand the impact of these design variables on the process and to understand their impact on reliability. Because of the small bump pitch possible with the Au thermocompression process, a silicon interposer with through silicon vias (TSVs) was also designed and fabricated. Since no one foundry had the capability of providing Au plating capability and suitable RF TSV technology, a number of different foundries needed to be coordinated to fabricate the devices.

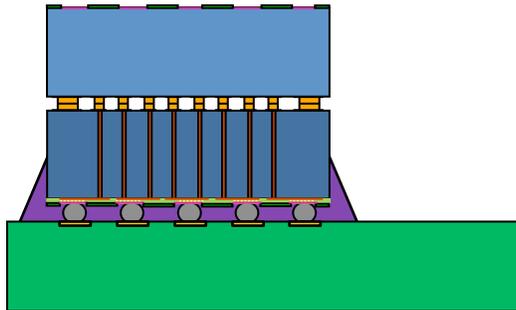
The interposer was fabricated to so that the SiGe chip could be flip chip attached with an Au-Au flip chip thermocompression process. The other side of the interposer had an array of solder flip chip pads that

facilitated attachment to a substrate. The interposer not only provided stress relief between the SiGe chip and the substrate, but the solder flip chip connection allowed for a possible rework scenario should one of the chip stacks in the array need to be replaced.

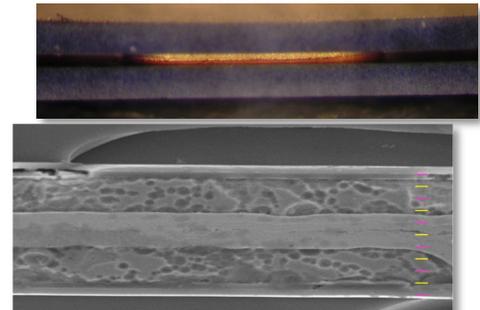
The process began with the fabrication of TSVs in the intrinsic silicon interposer wafer. Metal traces were formed on both sides to distribute the interconnections and to provide flip chip bond pads. Suitable under-bump-metallization was deposited and gold was plated on the seal ring and bump pads on the top-side of the interposer so that a suitable thermocompression bond interface was created. The SiGe chips were Au stud bumped and thermocompression bonded to the interposer wafer to form electrical interconnections as well as a hermetic seal ring around the flip chip bumps. The wafer was then precision diced to allow the die to be tiled into an array on the substrate. A solder flip chip process was used along with a standard solder underfill material. The array of devices was then subjected to a variety of electrical and reliability tests to understand the electrical performance of the array as well as the robustness of the assembly to extreme environmental conditions. These results were analyzed with respect to the design and process variables to understand the limits of each in designing products using this assembly technology.



A portion of the layout of the interposer wafer with Au flip chip pads and integral seal ring.



A cross section drawing of the SiGe die, Au flip chip bumps and interposer mounted to a substrate.



A side view and cross section of the hermetic seal ring around the flip chip

RESULTS: The Au-Au thermocompression flip chip process with integral hermetic seal rings passed all electrical and environmental stress tests. The Au flip chip bumps proved to be electrically superior and the seal ring not only provided protection from contamination, but it also provided a Faraday shield around the RF signal path. The silicon interposer with TSVs provided the suitable interface to the substrate and the die stack was able to be tiled into an array that emulated the phased-array antenna system. Design, material and process tradeoffs were understood in such a manner that allowed the technology to be applied to a number of different product applications.